

# Single-Event Transients in High-Speed Comparators<sup>†</sup>

A. H. Johnston, T. F. Miyahira and F. Irom

Jet Propulsion Laboratory  
California Institute of Technology  
Pasadena, California

## I. INTRODUCTION

Single-event transients are produced in linear integrated circuits when they are exposed to heavy ions or protons, and those transients can be a significant problem for electronic circuits in spacecraft [1-8]. Transients in comparators are usually the most difficult issue because they typically drive digital circuits that can potentially be upset by short-duration pulses, depending on the circuit application. Comparator transients are also more strongly dependent on circuit conditions than transients in other types of linear devices. For example, the probability of a high-level transient in deep space from the LM139 comparator is about three orders of magnitude higher for circuit applications with low differential input voltage ( $\approx 50$  mV) compared to applications with differential input voltage greater than 1 V [5].

Extensive work has been done on transients in moderate-speed comparators such as the LM139 (*response time 0.3 to 1.3  $\mu$ s*) that use substrate pnp and lateral pnp transistors [3-7]. However, little work has been done on high-speed comparators, which use different fabrication technologies and can respond more quickly to lower amounts of deposited charge. Evaluation of transients in linear circuits is a difficult issue because there are many interdependent variables. Differential input voltage, output loading, power supply voltage and the criterion used for defining significant output transients all affect the results.

This paper presents test results and analyses of transients in three types of high-speed comparators, shown in Table 1. The devices represent various technologies, with markedly different switching speeds and circuit designs. The increased switching speed of these devices requires higher internal operating currents, which is clearly seen from the input bias current specifications.

The LM119 is fabricated entirely with npn transistors but it is an older design, requiring negative as well as positive power supplies. The AD790 uses an advanced linear process that incorporates high-speed vertical pnp as well as standard npn devices; this requires more elaborate processing steps compared to the processing used for older linear designs, such as the LM139. The CMP401 uses a BiCMOS process with far lower power consumption, providing improved switching time performance compared to the other devices. It uses vertical pnp transistors along with lateral npn transistors. The vertical transistors are obtained by adding additional processing steps to the CMOS process. The lateral npn transistors have much better performance than the lateral pnp transistors in older bipolar designs. As shown in Figure 1, the CMP401 uses lateral transistors in a common-base configuration to improve the frequency response. They are also used as current mirrors (which are essentially equivalent to a common-base circuit), as well as in an emitter-follower stage that drives the output stage.

Table 1. Properties of the High-Speed Comparators Used in the Study

Device	Manufacturer	Technology	Input Bias Current	Switching Speed	Power Supply	Single-Ended Operation	Output Stage
LM119	National	"Old" linear bipolar	150 nA	80 ns	$\pm 5$ to $\pm 15$ V	no	Open collector
AD790	Analog Devices	Complementary bipolar	2.7 $\mu$ A	45 ns	+5 to $\pm 15$ V	yes	Active bipolar
CMP401	Analog Devices	BiCMOS	3 $\mu$ A	23 ns	+3 to $\pm 6$ V	yes	Active CMOS

<sup>†</sup>The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronic Parts and Packaging Program (NEPP), Code AE.

These circuit techniques allow fast switching speed to be obtained, even when lateral transistors are used within the circuit.

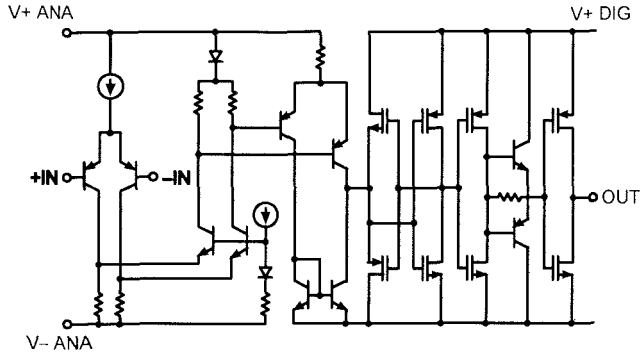


Figure 1. Simplified schematic for the CMP401 BiCMOS comparator. The npn devices in this process are lateral transistors.

Devices were tested with heavy ions at Brookhaven National Laboratory. Several ion species were used, with ranges from 120 to 37  $\mu\text{m}$ . Up to four different input voltage conditions were used, from 50 mV to 1 V. All tests were done with the devices in the “1” output state. Outputs were loaded with a 1k resistor. A five-volt power supply was used for all three device types, establishing a digital output drive of approximately 5 V. A negative power supply voltage was also required for the LM119 because of its design, but that does not affect the logic output swing. A high-speed line driver was connected to the output with a load capacitance of 10 pF. Output transients were captured with a Tektronix TDS700 oscilloscope, and stored on a computer for later analysis. The threshold level for transient capture was  $-200$  mV, even though few circuit applications would be affected by such small transients. The stored waveforms were examined after testing, applying an output voltage criterion of  $-3$  V which exceeds the typical noise margin of a TTL or CMOS circuit, and is a more useful criterion for most circuit applications of comparators.

## II. TEST RESULTS

### A. LM119 (Split Supply, Open Collector)

The cross section for  $-3$  V transients for the LM119 is shown in Figure 2. These results differ from those reported by Koga, et al. [3], clearly showing a dependence on differential input voltage that was not observed in the earlier tests.\* This may be due to the lower circuit voltage (5 V vs. 12 to 15 V in the tests of Koga, et al.) along with the lower capacitive loading in

\*The data from Koga, et al. are different only because of the application conditions that used during testing, not because of any technical oversight. This illustrates the complexity of evaluating transients in comparators. It is nearly impossible to encompass all operating conditions when tests of this nature are done.

our experiments. With  $\Delta V_{in} = 50$  mV, the threshold for  $-3$  V transients was about  $6 \text{ MeV-cm}^2/\text{mg}$ . Tests with higher differential input voltage increased the threshold to about  $11 \text{ MeV-cm}^2/\text{mg}$  and decreased the saturation cross section by about an order of magnitude compared to results with  $\Delta V_{in} = 50$  mV.

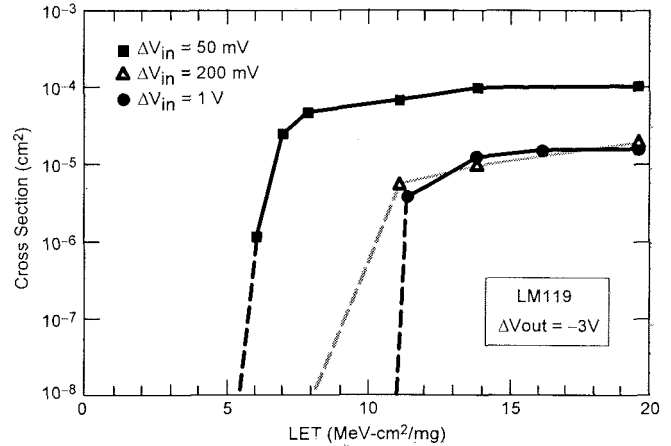


Figure 2. LM119 cross section vs. LET with various input voltages.

The distribution of transients is bimodal when the differential input voltage is low. Figure 3 shows histograms of the transient output voltage amplitude for  $\text{LET} = 11.2 \text{ MeV-cm}^2/\text{mg}$  with two different differential input voltage conditions. When  $\Delta V_{in}$  is increased to 200 mV the high-amplitude transients are suppressed, and the cross section is reduced.

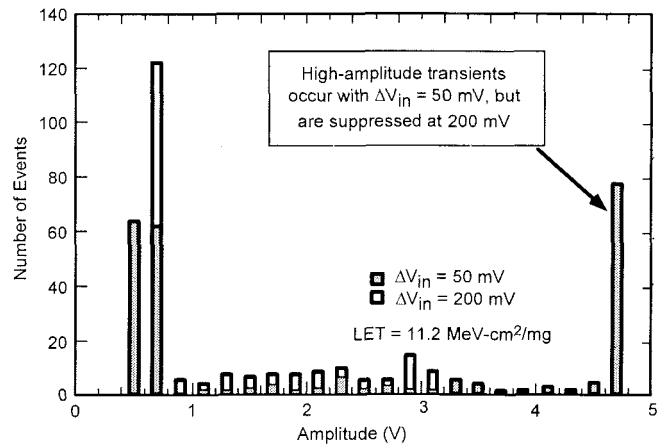


Figure 3. Histogram of output transient amplitudes showing suppression of high-amplitude transients when the differential input voltage is increased to 200 mV.

The mean width of the low amplitude transients is about 25 ns, compared to 42 ns for transients with high amplitudes. Rise times are typically a few nanoseconds.

### B. AD790 (Single Supply, Active Output)

The AD790 was quite sensitive to transients when it was tested with low  $\Delta V_{in}$ ; the threshold LET was about

3 MeV-cm<sup>2</sup>/mg, a factor of two lower than the threshold LET of the LM119. The threshold LET increased when  $\Delta V_{in}$  was increased to 200 mV, with a less abrupt dependence on LET. The cross section was also lower, as shown in Figure 3. In this figure results are shown for both high and low amplitude transients. Dashed lines show the cross section for a -200 mV threshold, while solid lines show the cross section for a -3V threshold for each condition.

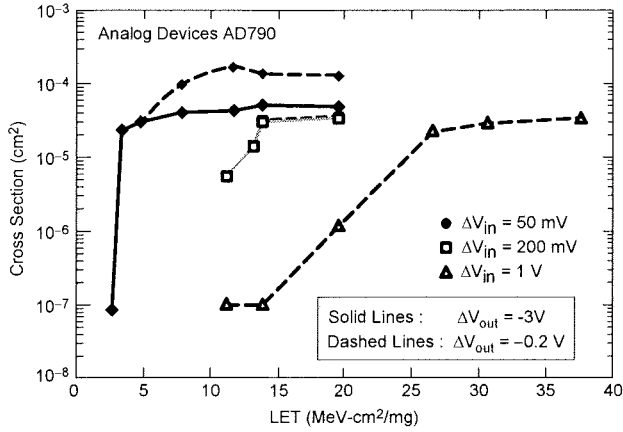


Figure 4. AD790 cross section vs. LET with various input voltages

With  $\Delta V_{in} = 1$  V, the device only exhibited very low amplitude transients, shown by the dashed line at the right (all transients for this input condition were less than -0.5 V). Even an LET of 37 MeV-cm<sup>2</sup>/mg did not produce enough charge to trigger the high-amplitude responses that occurred with lower input voltage conditions. This behavior was not observed for either of the other two device types.

### C. CMP401 (Single Supply BiCMOS, Active Output)

Results for the CMP01 are shown in Figure 5. The threshold LET with  $\Delta V_{in} = 50$  mV was nearly the same as that of the AD790, about 3 MeV-cm<sup>2</sup>/mg. However, the cross section of the CMP401 was less dependent on  $\Delta V_{in}$  than for either of the other comparators, which may be due to the BiCMOS design. There was also less difference in saturation cross section for low and high input voltage conditions. Those results suggest that the bipolar input stage has less effect on the overall response compared to the two types of bipolar comparators, and that other regions of the device are involved in many of the transients for the BiCMOS comparator.

A separate set of experiments was done using californium-252 in which the analog power supply voltage was reduced to 1 volt, effectively removing the high gain stage of the device (see Figure 1). The analog supply current was < 0.1 mA in this condition. The device still produced high-amplitude transients,

with a lower cross section, supporting the assumption that a large part of the overall response is due to the CMOS section of the device. It explains why the cross section is so high when the device is tested with large values of differential input voltage, unlike most other comparators. Tests done at the Brookhaven accelerator with reduced analog voltage condition showed that upsets did not occur.

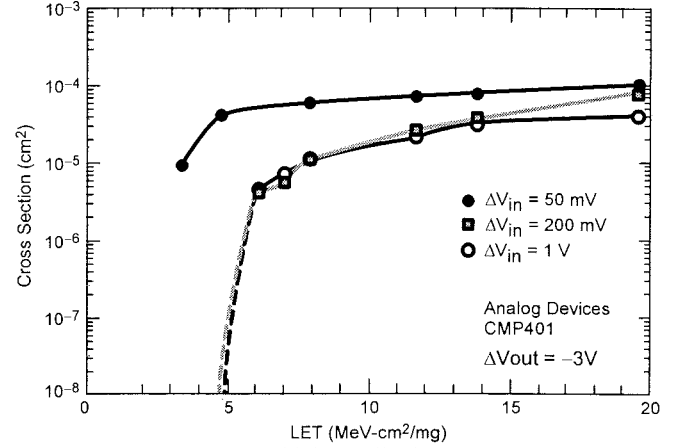


Figure 5. Cross section for high-amplitude output transients in the CMP401 BiCMOS comparator.

## III. DISCUSSION

In order to operate with higher switching speed, the input stages of high-speed comparators must operate at higher currents compared to low- and medium-speed comparators. For example, first-stage current of the LM119 is about 75  $\mu$ A, compared to 100 nA for the (much slower) LM139, an increase of nearly three orders of magnitude. There is a direct relationship between differential input voltage and the minimum conditions for upset. To first order, input stage inbalance for a basic differential input stage depends exponentially on differential input voltage. With  $\Delta V_{in} = 5$  mV, the current in the “off” transistor is 20% less than the current in the “on” transistor. In order for an ion strike to cause upset, current in the “off” device must increase by approximately 7.5  $\mu$ A. With  $\Delta V_{in} = 20$  mV, the threshold requirement increases to 25  $\mu$ A.

Consequently, direct charge collection from the ion strike is nearly always too low to cause high-level circuit transients, unless the device is operated with extremely low differential input voltage conditions, where the required current for upset is only a few microamps. The current must be collected in a time period that is comparable to the response time of the comparator, which is 80 ns for the LM119. Charge for upset for the above input conditions can then be estimated as 1.3, 4 and 11 pC for differential input voltages of 5, 20 and 60 mV.

Computer modeling of the pnp transistors that are used in the LM139 and LM111 showed that gain in the first-stage transistors was not important for LETs below about 15 MeV-cm<sup>2</sup>/mg [5]. However, they still responded to single-event transients at LETs as low as 3 MeV-cm<sup>2</sup>/mg. The mechanism for the response at low LET was charge from the collector to the substrate in the vertical pnp transistor, which does not have a buried layer. The charge was high enough to compete with the relatively low operating currents in the first stage, even without transistor amplification. That mechanism cannot occur for the high-speed comparators in this study because of the high operating currents, and, for the two bipolar devices, the presence of a buried layer that reduces direct charge collection by about an order of magnitude compared to bulk devices that extend into the substrate.

A basic differential amplifier is used at the input of all three comparators in this study. PISCES simulations were done to provide insight into the mechanisms for transient response from the first stage of these devices. A quasi-3D npn transistor model (radial symmetry) was used, running simulations with various values of forward voltage that correspond to different overdrive conditions for a differential transistor pair. Doping levels were determined from spreading resistance measurements. Figure 6 shows how charge in the collector, due to the effects of the ion strike, depends on LET and the differential input voltage. The ion was assumed to strike only one transistor in the dual transistor pair. Charge collected directly from the ion strike is less than 1 pC. The increase in charge is caused by multiplication of the small charge from the ion strike by transistor gain. The excess charge has a nonlinear dependence on

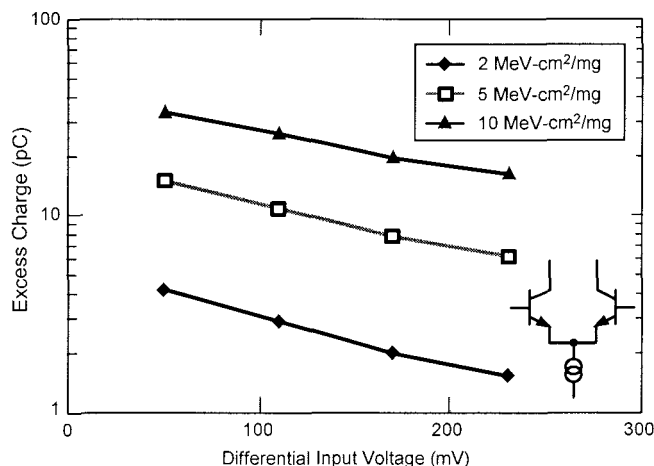


Figure 6. Modeling results for an npn transistor (with a buried layer) showing the effect of differential input voltage on excess charge collection.

differential input voltage, effectively making the critical charge for upset dependent on input voltage.

Figure 7 shows how charge in an npn transistor depends on emitter base voltage. To interpret this result, note that the “balance” point in a differential transistor pair corresponds to a forward voltage of about 620 mV. Thus, an emitter-base voltage of 0.6 mV corresponds to a differential input voltage of 20 mV. With LET = 2 MeV-cm<sup>2</sup>/mg the excess charge is about 2.5 pC, too low for the circuit to upset. However, an LET of 5 MeV-cm<sup>2</sup>/mg will provide an excess charge of about 10 pC, which exceeds current threshold requirements.

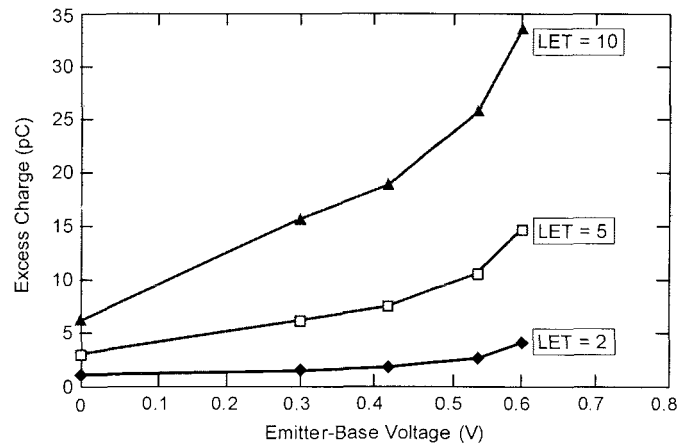


Figure 7. Dependence of excess charge on emitter-base voltage for a vertical npn transistor with a buried layer.

The time profile of the excess current must also be considered. Ions that strike the emitter produce a larger initial charge due to the ion shunt effect [9], which initiates the excess current mechanism within about 1 ns (that effect is difficult to test with lasers because the emitter region is often completely covered with metallization). Because of the shunt effect, the cross section is considerably lower for ions where the excess charge corresponds to the turn-on threshold; only ions that pass through the emitter will produce sufficient charge for upset. As LET is increased, then the cross section increases to the point where it corresponds to the entire area of the base, not just the region under the emitter. This is corroborated by comparing the area of the base region with the measured cross section of the device.

#### IV. CONCLUSIONS

This paper has discussed single-event transient responses of several types of high-speed comparators. Differential input voltage has a pronounced effect on their sensitivity to transients. For one device type,

SET sensitivity was completely eliminated (except for very low level transients) when  $\Delta V_{in}$  was increased from 200 mV to 1 V. The bimodal response for low values of differential input voltage shows that some response mechanisms are suppressed when the input stage is sufficiently overdriven.

Results for a BiCMOS comparator show less dependence on input conditions. Initial tests with the bipolar section effectively removed show that this is due to the CMOS section of the device, which can respond independently from the analog section.

The threshold LET and cross section of these high-speed comparators are not very different from comparators with lower response times. This is due to two competing effects: the lower critical charge is offset by lower charge collection within the more shallow structures of these devices, along with the higher operating currents.

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